

USB4 2.0 ENGINEERING CHANGE NOTICE FORM

Title: CLx Latency Tolerance Enhancement
Applied to: USB4 Specification Version 2.0

Brief description of the functional changes:

The minimal time at which the USB4 link is unavailable due to entry and exit to CL0s or CL1 latencies is well defined by a set of equations. There are applications which may tolerate longer CL0s or CL1 entry and exit latencies than the deterministic values dictated by these equations. This proposal provides an enhancement that allows a USB4 Port to be informed about longer CLx latency tolerances, using a new optional Port Operation.
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Benefits as a result of the changes:

USB4 Routers that adopt this change will be able to exit CL0s and CL1 using higher latencies than those strictly defined in the standard (when possible), and therefore will have better power saving opportunities

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
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NA

An analysis of the hardware implications:
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USB4 Routers and USB4 Re-Timers that implements this enhancement will need to support the new optional Port Operation.
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An analysis of the software implications:
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Optionally, implementing the software for the new Port Operation
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An analysis of the compliance testing implications:
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Conditionally, check USB4 Ports which implement this optional Port Operation.

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Actual Change

(a). Section 8.3.1.3.2 Get Capabilities (Conditional)

To Text:

Table 8-51. List of Capabilities

Capability Index	Capability Name	# of Data DWs returned	Default State	Reference
01h	Hot Plug Failure Indication	0	Disabled	Section 8.3.1.3.2.1
02h	Sequence bit in Notification Packet	0	Disabled	Section 8.3.1.3.2.2
03h	Buffer Allocation Per USB4 Port	0	Disabled	Section 8.3.1.3.2.3
<u>05h</u>	<u>CLx Latency Tolerance</u>	<u>0</u>	<u>Disabled</u>	<u>Section 8.3.1.3.2.5</u>
02h – FFh	Reserved	--		N/A

(b). Section 8.3.1.3.2.5 CLx Latency Tolerance

Add Text:

This capability allows USB4 Ports to use longer CL0s and CL1 exit times than defined in the standard.

This capability does not return any Data DWs.

(C). Section 8.3.2.5 Query CLx Latency Tolerance (Conditional)

Add Text:

A USB4 Port that supports CLx Latency Tolerance Capability shall support the Query CLx Latency Tolerance Port Operation.

The Query CLx Latency Tolerance Port Operation is used to collect the recommended CLx Latency Threshold entries reported for the USB4 Routers and USB4 Re-Timer on the link topology, supporting up to four entries. Each CLx Latency Threshold entry describes a recommended timing margin beyond which the port will bring additional power saving merit. A CLx Latency Threshold entry may optionally provide the expected power saving when used. Based on these entries, Software can create a distribution plan for the overall available CLx Exit latency margins between the different components on constructing the link topology.

Note: When the total resulting CLx Latency exceeds the value of tTrainingError, a port might initiate Gen4 Link Recovery in case Gen 4 Link Recovery Avoidance Supported is 0b, or in case it does not support CLx Latency Tolerance

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operation. It is then recommended for software to disable Gen 4 Link Recovery unless both router ports have Gen 4 Link Recovery Avoidance Supported set to 1b.

Operation Initiation

This Port Operation does not have Operation Data.

Operation Completion

Table 8-X describes the Completion Metadata for this operation.

Table 8-X

<u>DW</u>	<u>Bit(s)</u>	<u>Field Name and Description</u>
<u>0</u>	<u>15:0</u>	<p><u>CLx Exit Time Margin [1]</u> – This field contains a time value in microseconds. This value is the first out of four possible entries, representing a requested time addition for port's CL1 or CL0s exit time. Each threshold brings power saving merit in CL1 or CL0s states in increased order and may be considered by software to be applied (by setting <u>CLx Exit Time Margins</u> using the <u>Set CLx Latency Tolerance Port Operation</u>).</p> <p>A value of 00h for this field is illegal.</p>
<u>0</u>	<u>22:16</u>	<p><u>CL0s Power Saving Ratio [1]</u> – This field provides the percentage of additional CL0s power saving applied when <u>CLx Exit Time Margins</u> is set to be equal or higher than <u>CLx Exit Time Margin [1]</u>, using the <u>Set CLx Latency Tolerance Port Operation</u>. The savings are described with respect to PCL0s, the ports baseline power consumption at CL0s state. For a given PSR (Power Saving Ratio) the expected power consumption is given by $(1 - PSR) * PCL0s$.</p> <p>This field is optional. If unused shall be set to 00h. Allowed values:</p> <p>01h: Additional power saving of 1% when entering CL0s 02h: Additional power saving of 2% when entering CL0s ... 63h: Additional power saving of 99% when entering CL0s 64h-7F: Illegal values</p>
<u>0</u>	<u>23</u>	<u>Reserved</u>
<u>0</u>	<u>30:24</u>	<p><u>CL1 Power Saving Ratio [1]</u> – This field provides the percentage of additional CL1 power saving applied when <u>CLx Exit Time Margins</u> is set to be equal or higher than <u>CLx Exit Time Margin [1]</u>, using the <u>Set CLx Latency Tolerance Port Operation</u>. The savings are described with respect to PCL1, the ports baseline power consumption at CL1 state. For a given PSR (Power Saving Ratio) the expected power consumption is given by $(1 - PSR) * PCL1$.</p> <p>This field is optional. If unused shall be set to 00h. Allowed values:</p> <p>01h: Additional power saving of 1% when entering CL1 02h: Additional power saving of 2% when entering CL1 ... 63h: Additional power saving of 99% when entering CL1 64h-7F: Illegal values</p>

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<u>0</u>	<u>31</u>	Gen 4 Link Recovery Avoidance Supported – This field shall be set to 1b only for implementations that support avoiding the initiation of Gen 4 Link Recovery when exiting CLOs or CL1 due to a tTrainingError expiration. Otherwise, this field shall be set to 0b.
<u>1</u>	<u>15:0</u>	CLx Exit Time Margin [2] – This field contains a time value in microseconds. This value is the 2 nd out of the four possible thresholds as described for CLx Exit Time Margin [1] . This field is optional. If unused shall be set to 00h.
<u>1</u>	<u>22:16</u>	CL0s Power Saving Ratio [2] – This field provides the percentage of additional CLOs power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [1] .], similar to CL0s Power Saving Ratio [1]
<u>1</u>	<u>23</u>	Reserved
<u>1</u>	<u>30:24</u>	CL1 Power Saving Ratio [2] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [2] .], similar to Power Saving Ratio [1] .
<u>1</u>	<u>31</u>	Reserved
<u>2</u>	<u>15:0</u>	CLx Exit Time Margin [3] – This field contains a time value in microseconds. This value is the 3 rd out of the four possible thresholds as described for CLx Exit Time Margin [1] . This field is optional. If unused shall be set to 00h.
<u>2</u>	<u>22:16</u>	CL0s Power Saving Ratio [3] – This field provides the percentage of additional CLOs power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [3] .], similar to CL0s Power Saving Ratio [1]
<u>2</u>	<u>23</u>	Reserved
<u>2</u>	<u>30:24</u>	CL1 Power Saving Ratio [3] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [3] .], similar to CL1 Power Saving Ratio [1] .
<u>2</u>	<u>31</u>	Reserved
<u>3</u>	<u>15:0</u>	CLx Exit Time Margin [4] – This field contains a time value in microseconds. This value is the 4 th out of the four possible thresholds as described for CLx Exit Time Margin [1] . This field is optional. If unused shall be set to 00h.

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<u>3</u>	<u>22:16</u>	<u>CL0s Power Saving Ratio [4] – This field provides the percentage of additional CL0s power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [4]., similar to CL0s Power Saving Ratio [1]</u>
<u>3</u>	<u>23</u>	<u>Reserved</u>
<u>3</u>	<u>30:24</u>	<u>CL1 Power Saving Ratio [4] – This field provides the percentage of additional CL1 power saving applied when CLx Exit Time Margins is set to be equal or higher than CLx Exit Time Margin [4]., similar to CL1 Power Saving Ratio [1].</u>
<u>3</u>	<u>31</u>	<u>Reserved</u>

(d). Section 8.3.2.6 Set CLx Latency Tolerance (Optional)

Add Text:

A USB4 Port may optionally support the CLx Latency Tolerance Port Operation.

The CLx Latency Tolerance Port Operation is used to provide a USB4 Port extra timing margins to be used on any subsequent exit from CL0s or CL1. The provided CLx Exit Time Margins are the total extra time allowed for the USB4 Port to be distribute between the different transition states (or steps) beyond those defined in in **Table 4-72**.

A USB4 Port that implements this optional capability shall exit CL0s or CL1 within at most “CLx Exit Time Margins” beyond the time defined under Section 4.2.1.6.5 (**Equation 4-3 to Equation 4-10**). The port shall adhere to modifications to the CLx Exit Time Margins after being received (mainly considered after the values are reduced).

When the USB4 link disconnects, the “CLx Exit Time Margins” field returns to its default value (000h).

A port that operates in Gen 4 link rate shall not initiate Gen 4 Link Recovery in if both **Gen 4 Link Recovery Avoidance Supported** bit and **Gen 4 Link Recovery Avoidance Enabled** bit are set to 1b, and the tTrainingError timer expires when exiting CL0s or at Training state when exiting CL1 as defined in **4.2.1.6.5.4** and **4.2.1.6.5.1.2**.

A port that implements this port operation and runs at Gen 4 link rate may avoid invoking Gen 4 Link Recovery at the expiration of tTrainingError time when exiting CL0s or CL1, when setting CLx Exit Time Margins to any value other than 000h

This Port Operation does not have Operation Data. The Operation Metadata for the SET_CLX_LATENCY_TOL Port Operation is defined in Table 8-X.

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DW	Bit(s)	Field Name and Description
0	10:0	CLx Exit Time Margins – Sets the additional time margin budget for the USB4 Port to use when exiting CL0s and CL1. The value of this field: 000h: No timing margins are allowed (feature is disable). This is the default value. Other values define the number of microseconds that may be added to the CL0s and CL1 exit time budget for the source.
0	30:11	Reserved
0	31	Gen 4 Link Recovery Avoidance Enable 0b: The port may avoid the initiation of Gen 4 Link Recovery when exiting CL0s or CL1 due to a tTrainingError expiration if CLx Exit Time Margins was set to any value other than 000h (default) 1b: The port shall avoid the initiation of Gen 4 Link Recovery when exiting CL0s or CL1 due to a tTrainingError expiration. Enabling this bit has no impact if Gen 4 Link Recovery Avoidance Supported is set to 1b

(e). Table 8-64. List of Port Operations

To Text:

Port Operation	Opcode ¹	Operation		Completion		Reference
		Metadata DW	Data DWs	Metadata DW	Data DWs	
SET_TX_COMPLIANCE	TXCM (4D435854h)	1	0	0	0	Section 8.3.2.2.1
SET_RX_COMPLIANCE	RXCM (4D435852h)	1	0	0	0/1	Section 8.3.2.2.2
START_BER_TEST	SBER (52454253h)	1	0	0	0	Section 8.3.2.2.3
END_BER_TEST	EBER (52454245h)	1	0	0	2	Section 8.3.2.2.4
END_BURST_TEST	BBER (52454242h)	1	0	0	3	Section 8.3.2.2.5
READ_BURST_TEST	RBBER (52454252h)	1	0	0	3	Section 8.3.2.2.6
ENTER_EI_TEST	EEIT (54494545h)	1	0	0	0	Section 8.3.2.2.7
LFPS_TEST	LFPT (5450464Ch)	1	0	0	0	Section 8.3.2.2.8
SET_LINK_TYPE	LNKT (544B4E4Ch)	1	0	0	0	Section 8.3.2.2.9

¹ Byte 0 of the Opcode is the rightmost byte of the hexadecimal representation.

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ROUTER_OFFLINE_MODE	LSEN (4E45534Ch)	1	0	0	0	Section 8.3.2.3.1
ENUMERATE_RE-TIMERS	ENUM (4D554E45h)	0	0	0	0	Section 8.3.2.3.2
FEC_ERRORS_STAT	FERS (53524546h)	1	0	0	7	Section 8.3.2.3.3
READ_LANE_MARGIN_CAP	RDCP (50434452h)	0	0	0	3	Section 8.3.2.4.1
RUN_HW_LANE_MARGINING	RHMG (474D4852h)	1	0	0	2	Section 8.3.2.4.2
RUN_SW_LANE_MARGINING	RSMG (474D5352h)	1	0	0	1	Section 8.3.2.4.3
READ_SW_MARGIN_ERR	RDSW (57534452h)	0	0	1	0	Section 8.3.2.4.4
SET_TX_COMPLIANCE	TXCM (4D435854h)	1	0	0	0	Section 8.3.2.2.1
SET_RX_COMPLIANCE	RXCM (4D435852h)	1	0	0	0/1	Section 8.3.2.2.2
START_BER_TEST	SBER (52454253h)	1	0	0	0	Section 8.3.2.2.3
END_BER_TEST	EBER (52454245h)	1	0	0	2	Section 8.3.2.2.4
<u>QUERY_CLX_LATENCY_TOL</u>	<u>SCLT</u>	<u>1</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>Section 8.3.2.5</u>
<u>SET_CLX_LATENCY_TOL</u>	<u>QCLT</u>	<u>0</u>	<u>0</u>	<u>4</u>	<u>0</u>	<u>Section 8.3.2.6</u>

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Actual Change (USB4 Re-Timer Specification)

(f). Table 5-1 Port Operation Supported by a Re-timer (Required)

To Text:

Port Operation	Opcode ²	Operation		Completion		Reference
		Metadata DW	Data DWs	Metadata DW	Data DWs	
QUERY_LAST_RE-TIMER	LAST (5453414Ch)	0	0	1	0	Section 5.1.1
QUERY_CABLE_RE-TIMER	CBLR (524C4243h)	0	0	1	0	Section 5.1.2
SET_TX_COMPLIANCE	TXCM (4D435854h)	1	0	0	0	USB4 Specification
SET_RX_COMPLIANCE	RXCM (4D435852h)	1	0	0	0	USB4 Specification
ENTER_EI_TEST	EEIT (54494545h)	1	0	0	0	USB4 Specification
START_BER_TEST	SBER (52454253h)	1	0	0	0	USB4 Specification
END_BER_TEST	EBER (52454245h)	1	0	0	2	USB4 Specification
END_BURST_TEST	BBER (52454242h)	1	0	0	3	USB4 Specification
READ_BURST_TEST	RBER (52454252h)	1	0	0	3	USB4 Specification
SET_INBOUND_SBTX	LSUP (5055534Ch)	0	0	0	0	Section 5.2.1
UNSET_INBOUND_SBTX	USUP (50555355h)	0	0	0	0	Section 5.2.2
GET_NVM_SECTOR_SIZE	GNSS (53534E47h)	0	0	1	0	Section 5.2.3
NVM_SET_OFFSET	BOPS (53504F42h)	1	0	0	0	Section 5.2.4
NVM_BLOCK_WRITE	BLKW (574B4C42h)	0	16	0	0	Section 5.2.5
NVM_AUTH_WRITE	AUTH (48545541h)	0	0	1	0	Section 5.2.6
NVM_READ	AFRR (52524641h)	1	0	0	0 to 16	Section 5.2.7
READ_LANE_MARGIN_CAP	RDCP (50434452h)	0	0	0	2	USB4 Specification

² Byte 0 of the Opcode is the rightmost byte of the hexadecimal representation.

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RUN_HW_LANE_MARGINING	RHMG (474D4852h)	1	0	0	2	USB4 Specification
RUN_SW_LANE_MARGINING	RSMG (474D5352h)	1	0	0	0	USB4 Specification
READ_SW_MARGIN_ERR	RDSW (57534452h)	0	0	1	0	USB4 Specification
<u>SET_CLX_LATENCY_TOL</u>	<u>SCLT</u>	<u>1</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>USB4 Specification</u>
<u>QUERY_CLX_LATENCY_TOL</u>	<u>QCLT</u>	<u>0</u>	<u>0</u>	<u>1</u>	<u>0</u>	